Accelerating FPGA Designs and Design Work: Implementing Faster Designs Faster

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Current State of FPGA Use

- **Many FPGA researchers have begun questioning whether the moment for FPGAs has passed**
  - Use of co-processing units, such as graphical processing units, is becoming more common
- **Why?**
  - Design exploration is difficult
    - VHDL and Verilog are hard to use
    - Tools are painful to use
    - Simulation often does not match reality
    - Designers cannot predict what part of the algorithm matches the FPGA well
  - Designers are too focused on making any design work than making the best implementation of the design work
    - Fast design work often wins over better designs
- **Is it possible to get both fast designs and faster design work?**

Overview of Seminar

- **Fast FPGA designs:**
  - Miriam Leeser: Lessons on what to focus on and what to avoid
  - Bryan Penner: Improving FPGA speedup by matching the design to the architecture
  - Ray Andraka: Practical examples of insanely fast FPGA designs
- **Faster FPGA design work:**
  - Michael Wirthlin: An overview of the CHREC study on design work
  - George Harper: Improving both FPGA designs and design work through architectural exploration.
  - Tim Gallagher: Case studies of using higher order languages to do faster design work
- **Closing panel: Can we have both faster designs and faster design work or do we have to make a choice?**